IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Mark R. Thomann et al.

Title: METHOD AND APPARATUS FOR A HIGH SPEED CYCLICAL REDUNDANCY CHECK SYSTEM

Docket No.: [redacted]2US2

BOX PATENT APPLICATIONS
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

We are transmitting herewith the following attached items (as indicated with an "X"):

X A Divisional Patent Application comprising:
- X Communication entitled "Divisional Application Under 37 C.F.R. § 1.60" (3 pgs).
- X True and correct copy of prior application including specification (9 pgs), claims (3 pgs), Abstract (1 pg) and drawings (10 pgs).
- X A signed Combined Declaration and Power of Attorney (3 pgs).

X A Preliminary Amendment (5 pgs).
X A check in the amount of $770.00 to cover the Filing Fee.
X A return postcard
- Other: ___.

X The filing fee has been calculated below as follows:

CLAIMS AS FILED					
	(1) No. Filed		(2) No. Extra	Rate	Fee
BASIC FEE	XXXXX		XXXXX	XXXXX	$770.00
TOTAL CLAIMS	15 - 20	=	0	x 22 =	$0.00
INDEPENDENT CLAIMS	3 - 3	=	0	x 80 =	$0.00
FEE FOR MULTIPLE DEPENDENT CLAIMS PRESENTED					$0.00
TOTAL					$770.00

If the difference in Column (1) is less than zero, enter "0" in Column (2).

Please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-339-0331)

By: _____
Atty: Sheryl Sue Holloway
Reg. No. 37,850

CERTIFICATE UNDER 37 CFR 1.10:

"Express Mail" mailing label number: EM609376413US
Date of Deposit: April 17, 1997

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, BOX PATENT APPLICATIONS, Washington, D.C. 20231.

By: _____
Name: Matthew Hollister

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket Number	Anticipated Classification		Prior Application	
	Class	Subclass	Examiner	Art Unit
303.012US2			T. Brown	2306

DIVISIONAL APPLICATION UNDER 37 C.F.R. § 1.60

BOX PATENT APPLICATIONS
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This is a request for filing a divisional application under 37 CFR § 1.60 of Serial No. 08/474,397, filed on June 7, 1995 and entitled METHOD AND APPARATUS FOR A HIGH SPEED CYCLICAL REDUNDANCY CHECK SYSTEM.

1. X Enclosed is a true and correct copy of the prior application; including the specification, claims, drawings, oath or declaration showing the applicant's signature, and any amendments referred to in the oath or declaration filed to complete the prior application. (It is noted that no amendments referred to in the oath or declaration filed to complete the prior application introduced new matter therein.)

2. X Cancel in this application original claims 1-7 and 9-10 of the prior application before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

3. X The inventors of the invention being claimed in this application are:

(1) Mark R. Thomann
3608 Riva Ridge
Boise, ID 83709
Citizen of United States of America

(2) Huy Thanh Vo
2463 E. Red Cedar Lane #103
Boise, ID 83705
Citizen of United States of America

(3) Charles L. Ingalls
982 West Pennwood
Meridian, ID 83642
Citizen of United States of America

4. X Enclosed is a Preliminary Amendment (5 pages). Any additional fees for claims added in this Preliminary Amendment have been included in the filing fee as calculated below:

CLAIMS AS FILED					
	(1) Number Filed		(2) Number Extra	Rate	Fee
TOTAL CLAIMS	15 - 20	=	0	x 22	$0.00
INDEPENDENT CLAIMS	3 - 3	=	0	x 80	$0.00
FEE FOR MULTIPLE DEPENDENT CLAIMS PRESENTED					$0.00
BASIC FILING FEE					$770.00
				TOTAL FILING FEE	$770.00

If the difference in Column (1) is less than zero, enter "0" in Column (2).

5. X A check in the amount of $770.00 is attached to pay the filing fee.

6. X **The Commissioner is hereby authorized to charge any additional fees which may be required in connection with this application or credit any overpayment to Deposit Account No. 19-0743.**

7. X Amend the first sentence of the specification as follows:
"This application is a division of U.S. Patent Application Serial No. 08/474,397, filed June 7, 1995."

8. __ Informal drawings (__ sheets) are enclosed.

9. X The prior application is assigned of record to:

Micron Technology, Inc. .

10. X The Power of Attorney in the prior application is to:

SCHWEGMAN, LUNDBERG & WOESSNER, P.A. .

11. __ A petition and fee was filed on __ to extend the term in the parent application until ___.

Address all future communications to: (may only be completed by attorney or agent of record)

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, Minnesota 55402
Attn: Sheryl Sue Holloway
(Telephone: (612) 373-6939)

Date: April 17, 1997

Sheryl Sue Holloway
Reg. No. 37,850

"Express Mail" mailing label number EM609376413US

Date of Deposit April 17, 1997

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to Box Patent Applications, Assistant Commissioner for Patents, Washington, D. C. 20231

Matthew Hollister
printed name

signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Mark R. Thomann et al.	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.012US2
Title:	METHOD AND APPARATUS FOR A HIGH SPEED CYCLICAL REDUNDANCY CHECK SYSTEM	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Please amend claim 8 as follows:

8. (Amended) A method for cyclical redundancy check error generation in a system having a cyclical redundancy check generator, a data latch, and a data buffer connected by a plurality of data bus lines, the data latch having a precharge circuit and the data buffer having data buffer outputs, the method comprising the steps of:

inhibiting the cyclical redundancy check generator and the data buffer outputs;

precharging the plurality of data bus lines to a first logic level until a cyclical redundancy check strobe is detected;

turning off the precharge circuit;

activating the data buffer outputs to modulate charge on the plurality of data bus lines;

waiting for a sufficient time for the plurality of data bus lines to develop a charge differential;

latching data on the plurality of data bus lines [on] in the data latch; and

performing a cyclical redundancy check on the data latched [by] in the data latch.

Please add claims 11-24 as follows:

11. (New) The method of claim 8, further comprising the step of isolating the data latch from the plurality of data bus lines after the data is latched in the data latch.

12. (New) The method of claim 8, wherein the step of inhibiting the cyclical redundancy

check generator comprises the step of precharging the cyclical redundancy check generator to a second logic level.

13. (New) The method of claim 8, wherein an check word buffer is connected to the cyclical redundancy check generator and the step of performing the cyclical redundancy check comprises the steps of:

activating the cyclical redundancy check generator when the cyclical redundancy check strobe is detected;

generating an error check word from the data latched in the data latch; and

comparing the error check word with data in the check word buffer.

14. (New) A method for cyclical redundancy check error generation in a system having a cyclical redundancy check generator, a data latch, and two data buffers connected by a plurality of data bus lines, the data latch having a precharge circuit, and the data sources having data outputs, the method comprising the steps of:

inhibiting the cyclical redundancy check generator and the data outputs;

precharging the plurality of data bus lines to a first logic level until a cyclical redundancy check strobe is detected;

turning off the precharge circuit;

activating the data outputs from one of the data buffers to modulate charge on the plurality of data bus lines;

waiting for a sufficient time for the plurality of data bus lines to develop a charge differential;

latching data on the plurality of data bus lines in the data latch; and

performing a cyclical redundancy check on the data latched in the data latch.

15. (New) A programmable error detection and correction system comprising:

an error check module programmable for generating and comparing error check words;

a first parallel data bus programmable for transferring data from an edit buffer to a first data port;

a second parallel data bus programmable for transferring data from the first data port to the error check module and to the edit buffer, and further programmable for transferring data from the edit buffer to the error check module;

a third parallel data bus programmable for transferring an error check word between the error check module and the edit buffer;

a control module for programming the first, second and third data buses, and the error check module to operate according to a plurality of error processing modes.

16. (New) The programmable error detection and correction system of claim 15, wherein a first error processing mode causes the control module to program the second data bus to transfer data from the edit buffer to the error check module, causes the control module to program the third data bus to transfer a first error check word from the edit buffer to the error check module, and causes the error check module to generate a second error check word based on the data and to compare the first and second error check words.

17. (New) The programmable error detection and correction system of claim 15, wherein a second error processing mode causes the control module to program the second data bus to transfer data from the first data port to the edit buffer and to the error check module, causes the control module to program the error check module to generate an error check word from the data, and causes the control module to program the third data bus to transfer the error check word to the edit buffer.

18. (New) The programmable error detection and correction system of claim 15, wherein a third error processing mode causes the control module to program the first data bus to transfer first data from the edit buffer to the first data port, and causes the control module to program the second data bus to transfer second data from the first data port to the edit buffer.

19. (New) The programmable error detection and correction system of claim 15, wherein the edit buffer comprises two data portions and the control module programs the first and second buses to transfer data to and from the data portions according to a plurality of data protocols.

20. (New) The programmable error detection and correction system of claim 19, wherein a first data protocol stores a header word in one of the data portions and raw data in the other data portion.

21. (New) The programmable error detection and correction system of claim 19, wherein a second data protocol stores header data in one of the data portions and prepend and postpend data in the other data portion.

22. (New) The programmable error detection and correction system of claim 19, wherein a third data protocol stores raw data in both data portions.

23. (New) The programmable error detection and correction system of claim 15, wherein the error check module generates and compares cyclical redundancy check words.

24. (New) The programmable error detection and correction system of claim 15, wherein the control module programs a fourth parallel data bus to transfer data between a second data port and the edit buffer.

Respectfully submitted,

MARK R. THOMANN ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6939

Date April 17, 1997 By

Sheryl Sue Holloway
Reg. No. 37,850

"Express Mail" mailing label number EM609376413US

Date of Deposit. April 17, 1997

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents Washington, D.C. 20231

Printed Name Matthew Hollister

Signature

770-101 A

METHOD AND APPARATUS FOR A HIGH SPEED CYCLICAL REDUNDANCY CHECK SYSTEM

Field of the Invention

The present invention relates to digital cyclical redundancy check systems and, in particular, to a high speed cyclical redundancy check system for digital systems.

Background of the Invention

Digital systems often employ a cyclical redundancy check ("CRC") of data transferred by the system for error detection and correction of digital data. Present digital systems have error correction systems which generally require a fixed data transfer protocol to implement error detection and correction.

For example, in computer systems, data is transferred according to a predetermined protocol and a CRC is performed on each byte transferred. Raw data is passed through a CRC module which provides CRC bit information associated with each byte of raw data. This CRC bit information may be concatenated with the raw data and transferred with the raw data. The raw data and CRC bit information are then received. The CRC bit information is stored in a buffer and an error detection module performs another CRC on the raw data. If the newly generated CRC bit information matches the CRC bit information stored in the buffer, then the receiver has correctly received each bit of the raw data and there is no error correction necessary. If the CRC bit information does not match, then an error has been detected and the receiver can perform error correction accordingly.

For systems with small throughput, such error correction may be performed regularly on a fixed protocol, since the processing overhead of performing such correction is minimal. However, for systems with large data

volumes, the overhead of a fixed and inflexible error correction system may greatly impair throughput.

Additionally, some forms of digital data do not require error correction, since the information is required to be processed in real time and the loss of some of the raw data is not particularly detrimental to the operation of the system. One example is digitized speech applications. In this case, error correction is unnecessary overhead which diminishes throughput.

Therefore, there is a need in the art for a high speed error correction system. The error correction system should also be programmable, so that raw data passing through the system may optionally be checked or not checked as the situation demands. Such a system should be flexible to handle differing data protocols without having to perform hardware modifications.

Summary of the Invention

The present disclosure describes a system for cyclical redundancy checking of data in a digital computer system. The present system provides high speed error correction through the use of a programmable architecture. The system includes an input buffer, a latch, a CRC generator and write circuit, a status register, and an edit buffer which are connected on a common bus structure to provide maximum flexibility in performing error correction.

The data flow may be programmed to bypass the CRC module if the data does not require error correction. Additionally, the raw data may be processed to accomodate different data protocols, so that the system is not restricted to a single data protocol.

Brief Description of the Drawings

In the drawings, where like numerals describe like components throughout the several views:

Figure 1 is a block diagram of one embodiment of a cyclical redundancy check system;

Figure 2A and Figure 2B and Figure 2C are a detailed schematic of the cyclical redundancy check system of Figure 1;

Figure 3 is a detailed schematic of one example of a CRC generator module for the cyclical redundancy check system of Figure 1;

Figure 4 is a detailed schematic of one stage of the CRC generator module of Figure 3;

Figure 5A and Figure 5B are a detailed schematic of one example of a compare circuit for the cyclical redundancy check system of Figure 1;

Figure 6 is a detailed schematic of one example of a latch circuit for the cyclical redundancy check system of Figure 1; and

Figure 7 is a flow diagram showing one example of a single cycle operation of the cyclical redundancy check system of Figure 1.

Detailed Description of the Preferred Embodiment

In the following detailed description of the preferred embodiment, references are made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that structural changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present inventions is defined by the appended claims and equivalents thereof.

Figure 1 shows a general block diagram of one embodiment of the cyclical redundancy check (CRC) system. The data flow through the system is bidirectional. Data inputs into port IOD[0:31] on the left hand side of Figure 1 can transfer to ports HE[0:31], PP[0:31], and CRC Generator 130. Data from ports HE[0:31] and PP[0:31] can transfer to CRC Generator 130 via data bus 105 using gates 183 and 185, or data bus 106 using gates 184 and 186 for transfer to

port IOD[0:31] for output. Additionally, inputs into port IOD[0:31] may also be processed by the CRC system 100 and return to port IOD[0:31] for output. Similarly, inputs to ports HE[0:31] and PP[0:31] may be processed internally in CRC system 100 and returned to ports HE[0:31] and PP[0:31]. Therefore, the architecture of CRC system 100 is programmable and flexible to handle different protocols and data processing operations.

Data flow control through CRC system 100 is performed via control 190 by using inputs through gates 181-189, CRC enable 192, input enable 196, Dout Latch Enable 197, and status enable 194. Control 190 also receives error signal 198 for processing error correction information provided by CRC generator 130, edit buffer 160, and compare 170.

Modes of Operation

The improved architecture of the present invention provides flexibility in data flow and data processing which can be demonstrated by a number of processing modes. In a first mode of operation, CRC system 100 receives parallel data from ports C[0:7], HE[0:31], and PP[0:31] by enabling gates 187, 188, and 189, respectively. Data from these ports is entered into edit buffer 160 and stored there for further processing. The raw data stored in edit buffer 160 may be transferred using a number of different protocols, however, a frequently encountered protocol includes 8 bits of CRC information stored in register 160a of edit buffer 160, 32 bits of header information stored in register 160b, and 32 bits of raw data stored in register 160c. Another protocol includes 8 bits of CRC information stored in register 160a of edit buffer 160, 32 bits of header information stored in register 160b, and 32 bits of prepend and postpend data stored in register 160c. Figure 1 illustrates register 160a as 8 bits wide, 160b as 32 bits wide, and 160c as 32 bits wide, however, those skilled in the art will readily recognize that different register bit lengths may be employed without departing form the scope and spirit of the present invention. The use of these register lengths is not intended in an exclusive or limiting fashion.

In this first mode of operation, CRC system 100 is used to receive data from ports C[0:7], HE[0:31], and PP[0:31] and verify that the data received is error free. Data is stored in edit buffer 160 by strobing gates 187, 188, and 189. The gates shown in Figure 1 represent parallel transmission gates of 8, 32 and 32 bits, respectively. Data from either register 160b or register 160c may be transferred to CRC generator 130 over data bus 105 using gates 183 and 185. CRC generator 130 must be enabled by control 190 via CRC enable 192 to generate a new 8 bit CRC word based on the 32 bits presented to the input of CRC generator 130. CRC write circuit 132 latches the newly generated CRC word, which is then available to compare 170. The contents of register 160a are also provided to compare 170 upon strobing gate 182, and compare 170 generates error signal 198. Compare 170 generates a logic one if there is a difference in the CRC words from CRC generator 130 and register 160a. The protocol determines whether CRC checking is performed on the contents of register 160b or 160c, however, in this embodiment, the preference is to perform error correction on the contents of register 160b. The present CRC system 100 can generate CRC information for either data stored in register 160b or 160c, adding to the number of modes which may be processed by the present system.

In a second mode of operation, the present CRC system takes raw data from port IOD[0:31] and formats the data for transmission by (1) generating the appropriate CRC word for the raw data and transferring the CRC word to port C[0:7], and (2) transferring the raw data to port HE[0:31] or PP[0:31], depending on the protocol. In this second mode, the present CRC system 100 receives a 32 bit word into port IOD[0:31] and stores the word in latch 110 when input buffer 120 is activated with an input enable 196 from control 190. The protocol used determines which 32 bit port of edit buffer 160 receives the stored word (raw data). For example, in one operation, the stored word in latch 110 is sent to register 160b via data bus 105 by enabling gate 183. In another example, the stored word is sent to register 160c via data bus 105 an by enabling gate 185. If error correction is desired on the word in latch 110, the word is processed by

asserting a CRC enable 192 of CRC generator 130 for CRC word generation. The CRC word generated can be stored in register 160a by enabling gate 181.

A variation of this second mode of operation allows 64 bits of data to be processed by repeated strobes of 32 bit words. The first and second 32 words of the 64 bits are stored in edit buffer 160 by repeated latches of data from port IOD [0:31] into latch 110 and to registers 160b and 160c using data bus 105 and gates 183 and 185. In this case, however, CRC word generation must occur on only 32 bits of the 64 bit data. However, the flexibility of the present CRC system 100 allows the CRC to be programmed on either the 32 bit word stored in register 160b or register 160c.

In a third mode of operation CRC system 100 provides a "pipeline" flow between IOD[0:31] and HE[0:31] or PP[0:31]. Data flow is bidirectional, and may proceed from HE[0:31] and PP[0:31] to IOD[0:31]. Data from IOD[0:31] is transferred to HE[0:31] and PP[0:31] via input buffer 120, latch 110, data bus 105, and gates 183 and 185. Data from HE[0:31] and PP[0:31] is transferred to IOD[0:31] using data bus 106, Dout latch 140, and gates 184 and 186. Data can be pipelined in three different formats:

format 1 provides 32 bit transfer between IOD[0:31] and HE[0:31];

format 2 provides 32 bit transfer between IOD[0:31] and PP[0:31]; and

format 3 provides 64 bit transfer by successive 32 bit transfers between IOD[0:31] and both HE[0:31] and PP[0:31].

Note also that each of the above formats is doubled since each format may or may not require CRC on the data transferred. However, in the 64 bit format, CRC information can only be generated for 32 bits of the 64 bit word.

In yet another mode of operation, CRC system 100 provides 32 bit word transfer and CRC in a single cycle to maximize speed of data transfer. For example, assume edit buffer 160 contains a CRC word in register 160a, a header word in 160b, and raw data in 160c. In a single cycle (1) the raw data is transferred to Dout latch 140 via data bus 106 and gate 186, (2) the header word

is CRC error checked using data bus 105 and gate 183, and (3) compare 170 enabled and checks the CRC Generator 130 8 bit output against the 8 bit data in register 160a. Anytime an "output"operation is performed, the Dout-latch-enable 197 will activate Dout latch 140 and data will be presented to IOD[0:31].

The flexibility and programmability of the present CRC system 100 also provides a mode whereby the CRC can be performed on the contents of register 160c instead of 160b. In this mode, data bus 106 and gate 184 are used to transfer the contents of register 160b to Dout latch 140. Data bus 105 and gate 185 are used to transfer the contents of register 160c to CRC generator 130 for CRC word generation. CRC system 100 has a flexible architecture which provides other permutations of data transfer than those mentioned, and the modes demonstrated were not intended in an exclusive or limiting sense.

CRC system 100 allows a user to put data into the PP 160c or HE 160b registers and/or register 160a and at the same time read data from the status register 150 and present data onto bus 106 and into Dout latch 140 and out to IOD [0:31]. In alternate embodiments, status register 150 comprises separate subregisters, similar to edit buffer 160, and multiplexers to selectively connect each subregister to data bus 106.

One example of a single cycle operation is shown in Figure 7. In a single cycle, CRC system 100 takes data inputs on IOD[0:31] and latches them into latch 110 (steps 710, 720, and 730). The input buffer is disabled to prevent further data transitions from being transmitted to latch 110 from input buffer 120 (step 740). The data in latch 110 is driven onto data bus 105 (step 750). At this point the data is available for either register 160b or 160c via data bus 105 and gates 183 and 185, respectively (step 760). Other operations are performed in the same cycle, for instance, the contents of status register 150 may be transferred to IOD[0:31] using Dout latch 140 (steps 770, 780, 790, and 800). Other operations are possible without departing from the scope and spirit of the present invention. Coordination of the enable signals is performed by control 190. One embodiment of control 190 uses combinational logic and analog timing delays to synchronize

the timing of the enables used in the single cycle operation. Another embodiment uses a processor and digital timer to perform the control. Other methods of control are possible without departing from the scope and spirit of the present invention.

5

Detailed Logic Diagrams

Figure 2A and Figure 2B and Figure 2C are a detailed schematic of the CRC system of Figure 1, showing detailed logic diagrams for compare 170, latch 110, CRC driver 132, status register 150, Dout latch 140, and edit 10 buffer 160. Figure 3 is a detailed logic diagram of CRC generator 130. An exemplary stage 310 of CRC generator 130 is shown in Figure 4. Figure 5A and Figure 5B are a detailed logic diagram of one embodiment of compare circuit 170. Figure 6 is a detailed logic diagram of latch circuit 110.

15 High Speed CRC Operation

A high speed and compact CRC system 100 is produced from an advanced edit buffer 160 latch (EB_HFF 209 of Figure 2C) and a tri-state inverter 7 driver circuit 207 of Figure 2B. To generate the CRC either the data of register 160b or 160c are multiplexed onto data bus 105 (EBIO[0:31], or D 20 and C of Figure 2C) and strobed into CRC generator 130 using latch 110 (isosa_crc latches 110 of Figure 2A), which is shown in more detail in Figure 6. Each isosa_crc latch of latch 110 has precharge, isolation, strobe, and latch circuits. In the precharge time the lines of data bus 105 are precharged high, the CRC strobe 192 is low, and the edit buffer 160 is precharged. Upon a CRC 25 strobe 192, the precharge turns off and either the write driver or the edit buffer 160 outputs are activated to allow charge to be dumped onto data bus 105. A period of time sufficient to allow a charge differential to develop passes and the data is latched into the latch 110, which allows for precharge to be activated for the next access and saves power by isolating a large capacitance of the data bus 30 105 lines. At this point in time data is latched and presented at the Q and Q*

outputs of latch 110 and will remain valid until another access. The latch 110 Q and Q* outputs are at full CMOS value for the CRC generator 130, which uses a precharge scheme and requires stable DC inputs for proper activation. The CRC precharge is disabled to generate CRC outputs from CRC generator 130. This scheme is very fast and requires less layout space than a CMOS EXOR gate type of circuit.

Conclusion

Although specific embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent implementations calculated to achieve the same purposes may be substituted for the specific embodiment shown and described without departing from the scope of the present invention. For example, the number of bits per register may vary without departing from the scope and spirit of the present invention. Additionally, minor variations in the connections of the registers and buffers in the design may be performed without deviating from the present invention. Those with skill in the electrical, computer, and telecommunications arts will readily appreciate that the present invention may be implemented in a very wide variety of embodiments. For example, any digital system incorporating error correction may use the present invention to provide programmable error correction for enhanced throughput. This includes digital video, audio, computers, computer networks, and other telecommunications systems. This application is intended to cover any adaptations or variations of the preferred embodiment discussed herein. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

WE CLAIM:

1. An error correction system, comprising:

an input buffer, connected to a first port;

a latch, connected to the input buffer, for latching data;

an edit buffer having an error portion for storing an error correction word and a data portion for storing a data word;

an error word generator having an input and an output, the input connected to the latch and the output connected to the edit buffer, for generating an error word based on data in the latch;

a compare circuit, connected to the error word generator and the edit portion of the edit buffer, for generating an error signal based on the error word and the error correction word in the error portion of the edit buffer;

a first data bus, connecting the input of the error word generator to the data portion of the edit buffer; and

a second data bus, connecting the data portion of the edit buffer to an output latch and connecting the output latch to the first port;

wherein the edit buffer has an error word port for the error portion and a data word port for the data portion.

2. The error correction system of claim 1, wherein the data portion of the edit buffer comprises a header portion and a raw data portion and wherein the data word port has a header word port for the header portion and a raw word port for the raw word portion.

3. The error correction system of claim 1, wherein the data portion of the edit buffer comprises a header portion and a prepend data and postpend data portion and wherein the data word port has a header word port for the header portion and a prepend and postpend data port for the prepend data and postpend data.

4. The error correction system of claim 1, wherein the error word generator is a cyclical redundancy check generator.

5. The error correction system of claim 2, wherein the error word generator is a cyclical redundancy check generator.

6. The error correction system of claim 3, wherein the error word generator is a cyclical redundancy check generator.

7. A method for error detection and correction of a data word having a data portion, a header portion, and an error correction portion, comprising the steps of:

simultaneously transmitting the data portion to a latch and the header portion to an error signal generator;

generating an error signal from the error signal generator based on the header portion and the error correction portion;

if the error signal is negative, then enabling the latch to transmit the data word; and

if the error signal is positive, then disabling the latch to inhibit transmission of the data word.

8. A method for cyclical redundancy check error generation in a system having a cyclical redundancy check generator, a data latch, and a data buffer connected by a plurality of data bus lines, the data latch having a precharge circuit and the data buffer having data buffer outputs, the method comprising the steps of:

inhibiting the cyclical redundancy check generator and the data buffer outputs;

precharging the plurality of data bus lines to a first logic level until a cyclical redundancy check strobe is detected;

turning off the precharge circuit;

activating the data buffer outputs to modulate charge on the plurality of data bus lines;

waiting for a sufficient time for the plurality of data bus lines to develop a charge differential;

latching the plurality of data bus lines on the data latch; and

performing a cyclical redundancy check on data latched by the data latch.

9. A method for performing multiple operations in a single cycle in a cyclical redundancy check system, the system having a port, an input buffer, an input latch, a first data bus, a register, an output latch, and a second data bus, the method comprising the steps of:

activating the input buffer to receive data from the port;

latching data from the input buffer into the input latch;

disabling the input buffer;

transmitting data on the input latch to the first data bus; and

activating the output latch to transfer the contents of the second data bus to the port.

10. The method of claim 9, further comprising the steps of:

storing data on the first data bus in the register, and

processing data stored in the register.

METHOD AND APPARATUS FOR A HIGH SPEED CYCLICAL REDUNDANCY CHECK SYSTEM

Abstract

A high speed cyclical redundancy check system for use in digital systems. The high speed cyclical redundancy check system providing programmable error correction functions for different data protocols. The high speed cyclical redundancy check system providing programmable data paths for minimizing overhead and maximizing throughput. The system supporting multiple operations in a single cycle.

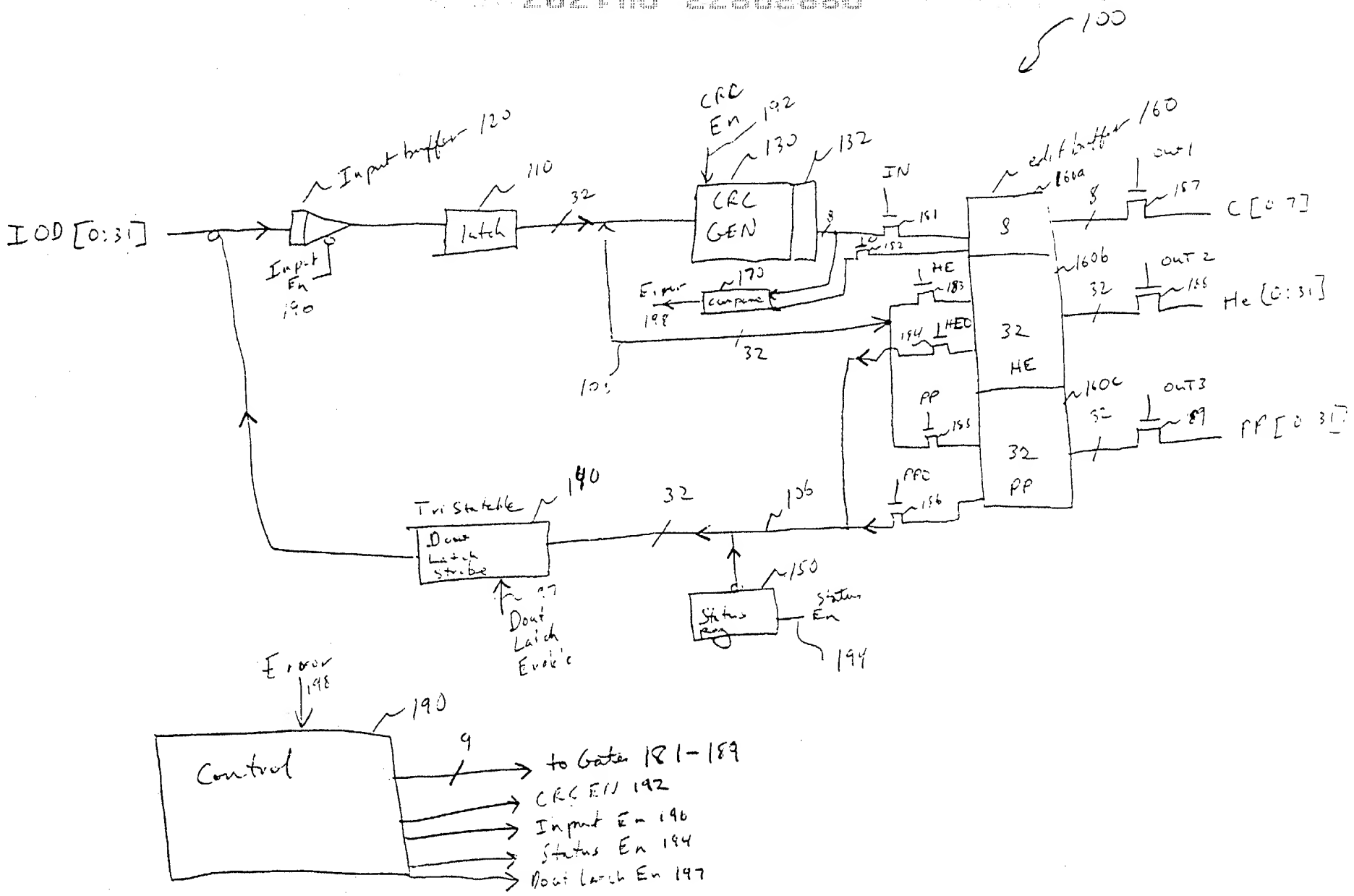

100
IOD [0:31]
Input buffer 120
Input En 190
110
Latch
32
CRC En 192
130
CRC GEN
132
8
IN
151
152
Error 198
170
Compare
HE
183
194
HEO
32
HE
PP
185
PP0
186
32
PP
edit buffer 160
160a
8
OUT1
187
C [0:7]
160b
32
OUT2
188
He [0:31]
160c
32
OUT3
189
PP [0:31]
101
32
Tri Statable
140
Dout Latch Strobe
197
Dout Latch Enable
106
32
150
Status Reg
Status En
194
Error
198
190
Control
9
to Gates 181-189
CRC En 192
Input En 196
Status En 194
Dout Latch En 197

FIG 1

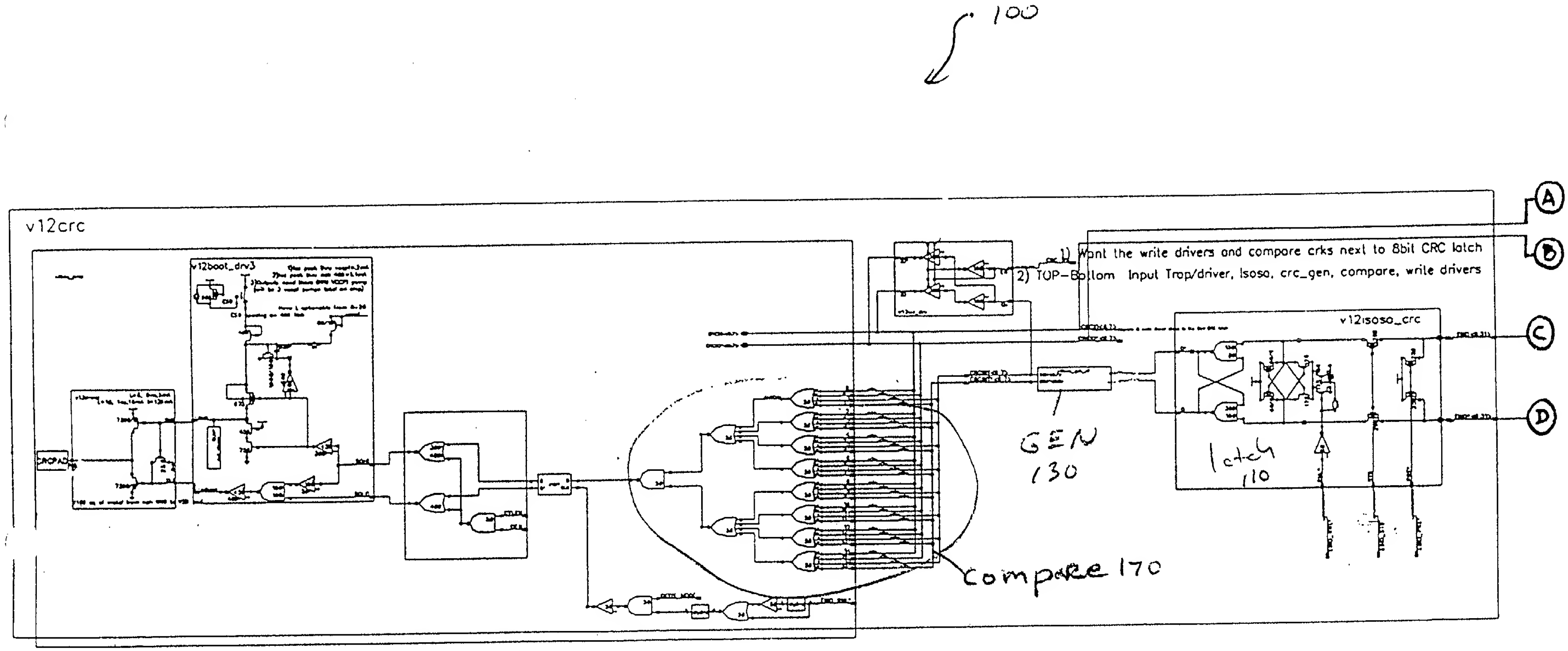

100
v12crc
v12boot_drv3
CRCPAD
1) Want the write drivers and compare crks next to 8bit CRC latch
2) TOP-Bottom Input Trap/driver, lsoso, crc_gen, compare, write drivers
v12isoso_crc
GEN 130
latch 110
Compare 170
A
B
C
D

FIG. 2A

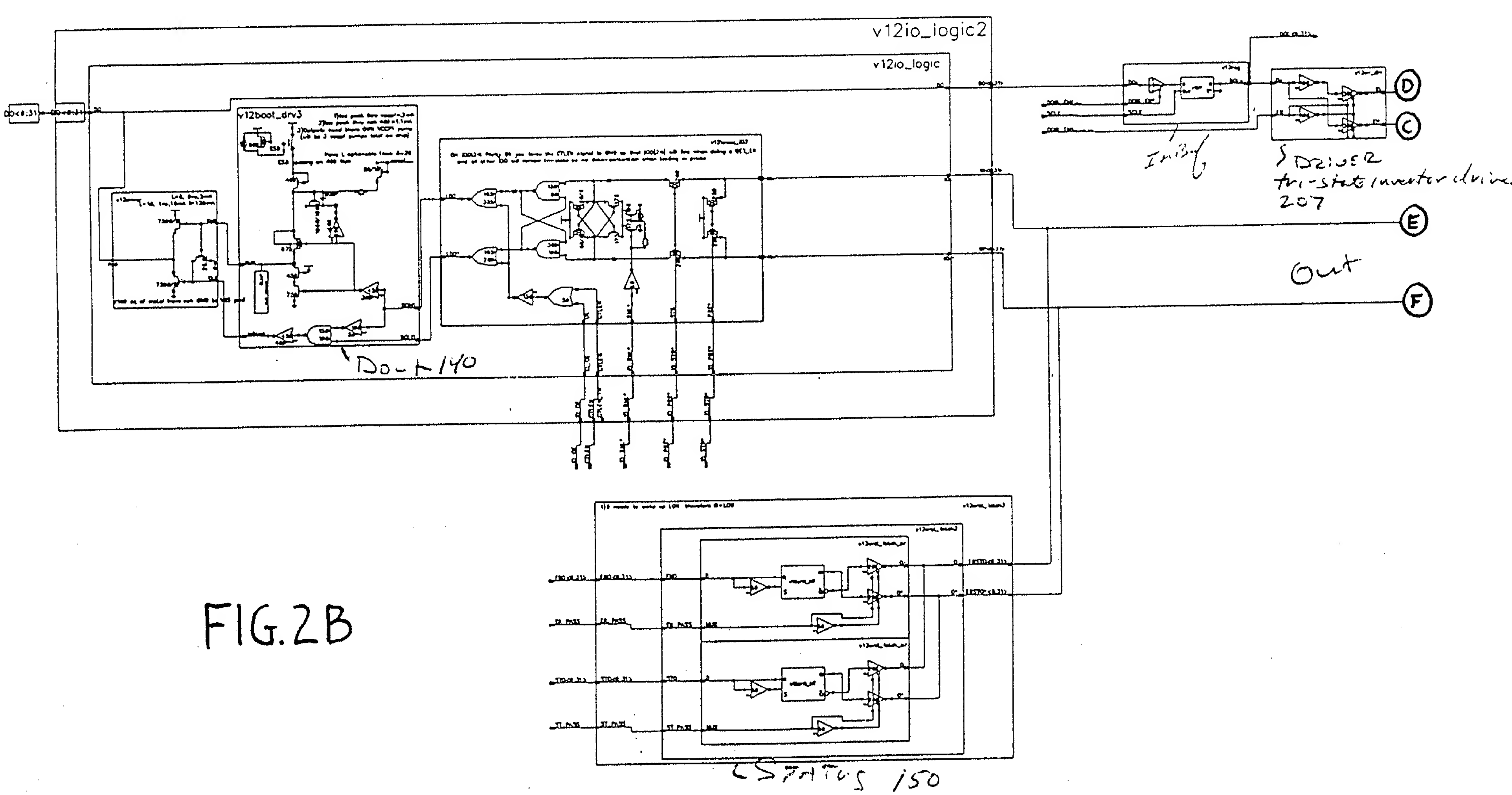

v12io_logic2
v12io_logic
v12boot_drv3
Dout 140
In Buf
Driver tri-state inverter driver 207
Out
Status 150
D
C
E
F

FIG.2B

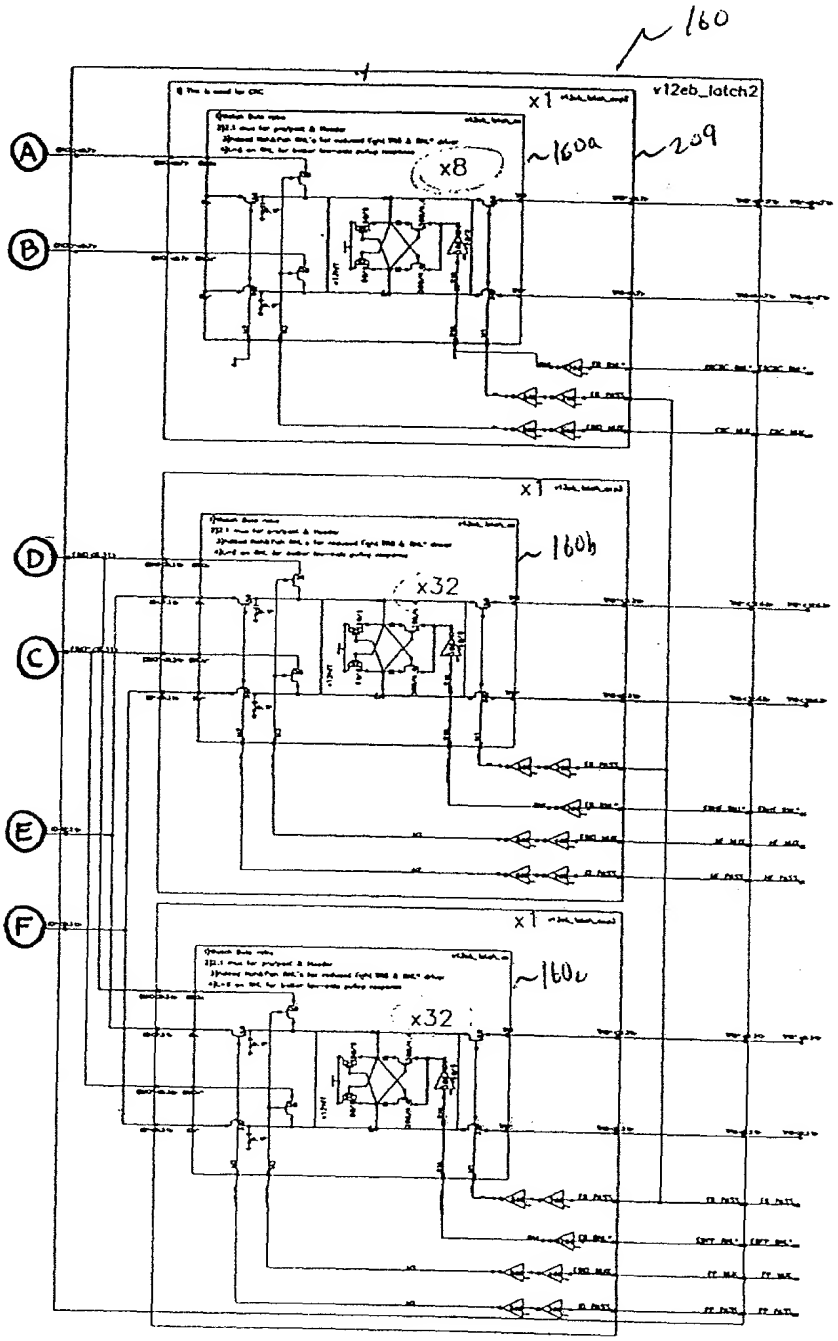
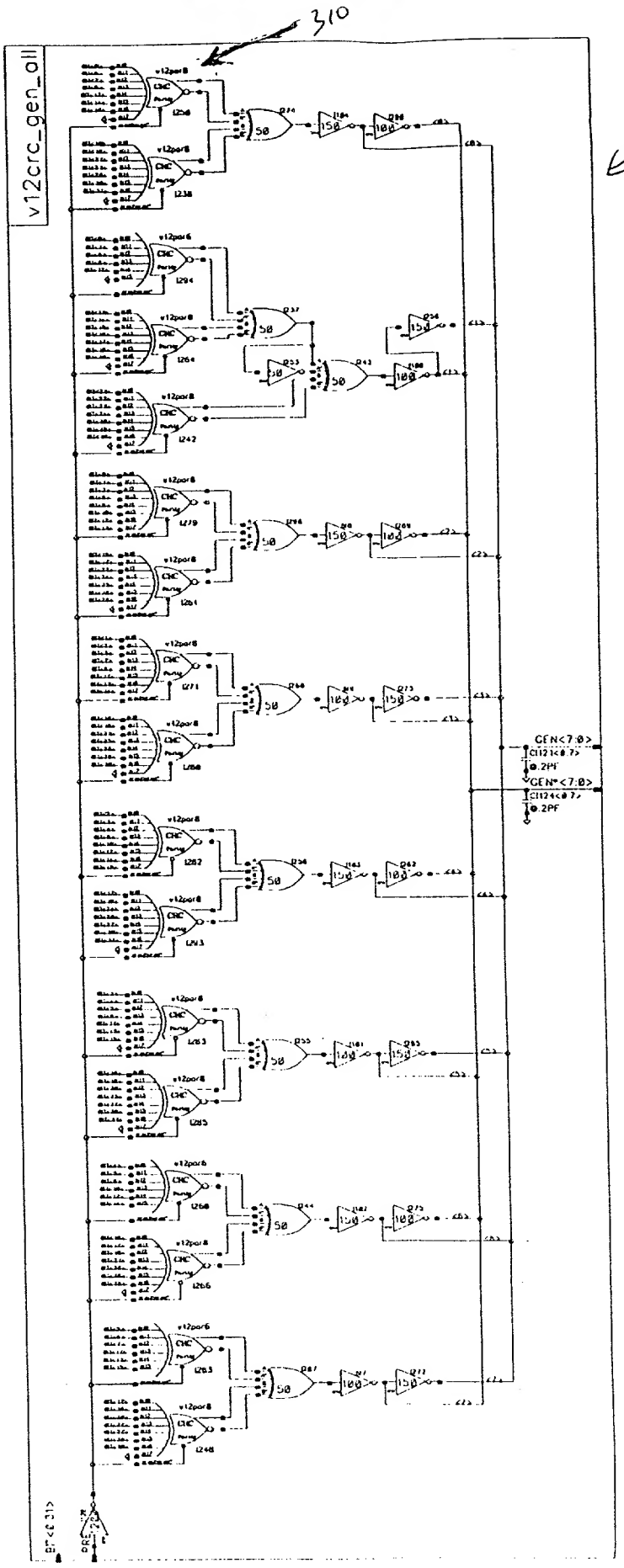
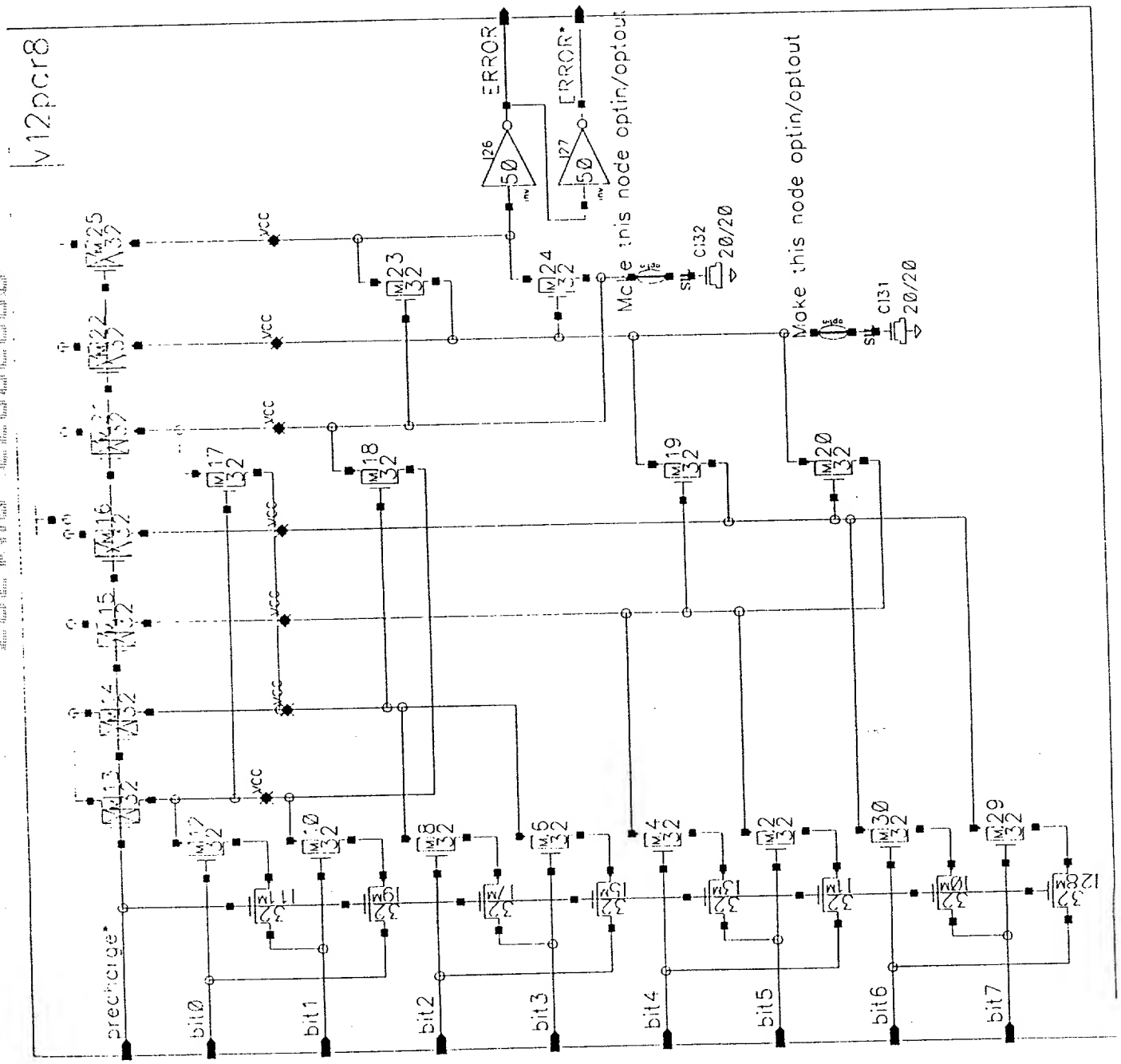


FIG. 2C


310
130
v12crc_gen_all
v12par8
CRC
Parity
50
100
150
GEN<7:0>
GEN*<7:0>
.2PF

F16 3

FIG 4


v12pcr8
ERROR
ERROR*
Make this node optin/optout
Make this node optin/optout
C132
20/20
C131
20/20
vcc
precharge*
bit0
bit1
bit2
bit3
bit4
bit5
bit6
bit7

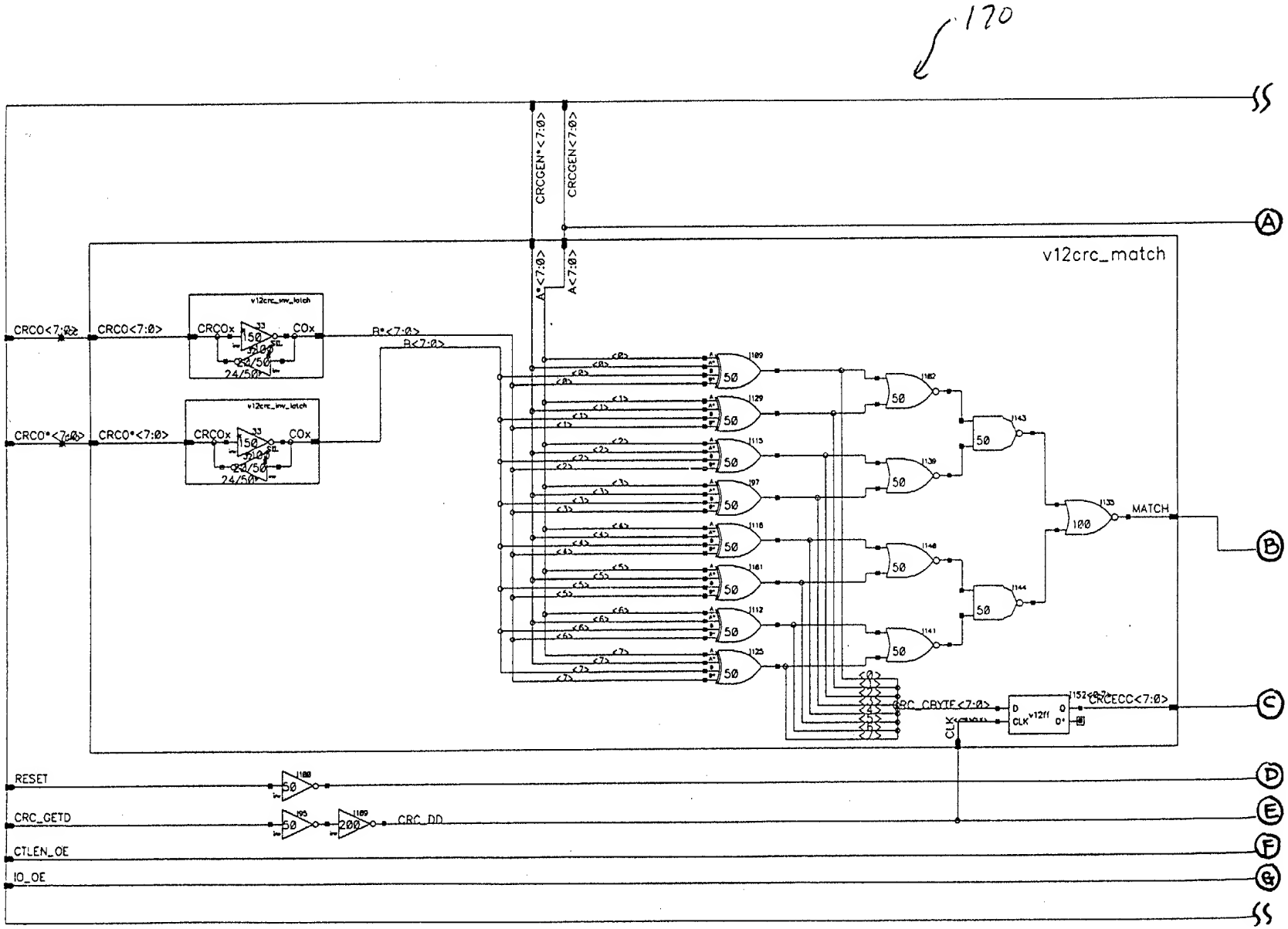

170
CRCGEN*<7:0>
CRCGEN<7:0>
A*<7:0>
A<7:0>
v12crc_match
CRCO<7:0>
CRCO*<7:0>
CRCOx
COx
B*<7:0>
B<7:0>
MATCH
CRC_CRYTE<7:0>
CRCECC<7:0>
CLK
RESET
CRC_GETD
CRC_DD
CTLEN_OE
IO_OE
A
B
C
D
E
F
G

FIG. 5A

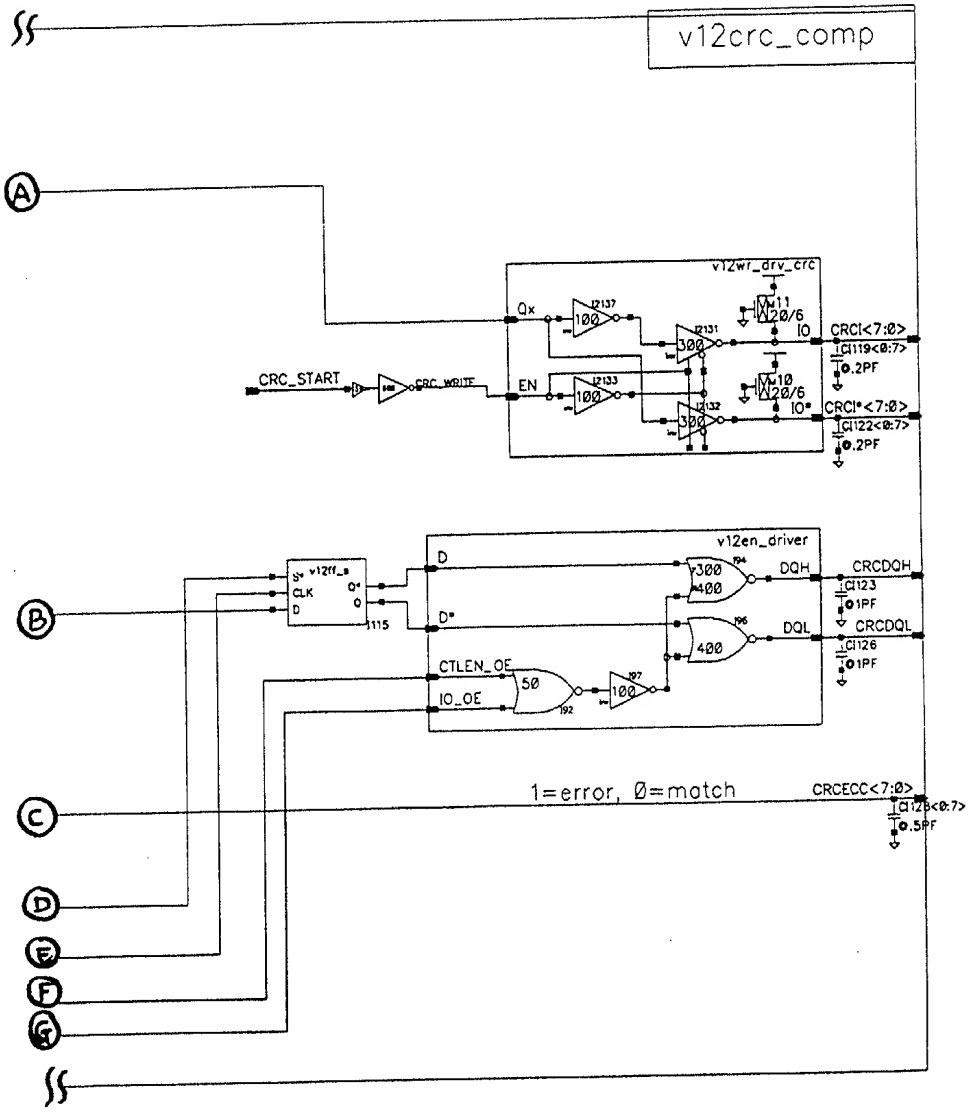
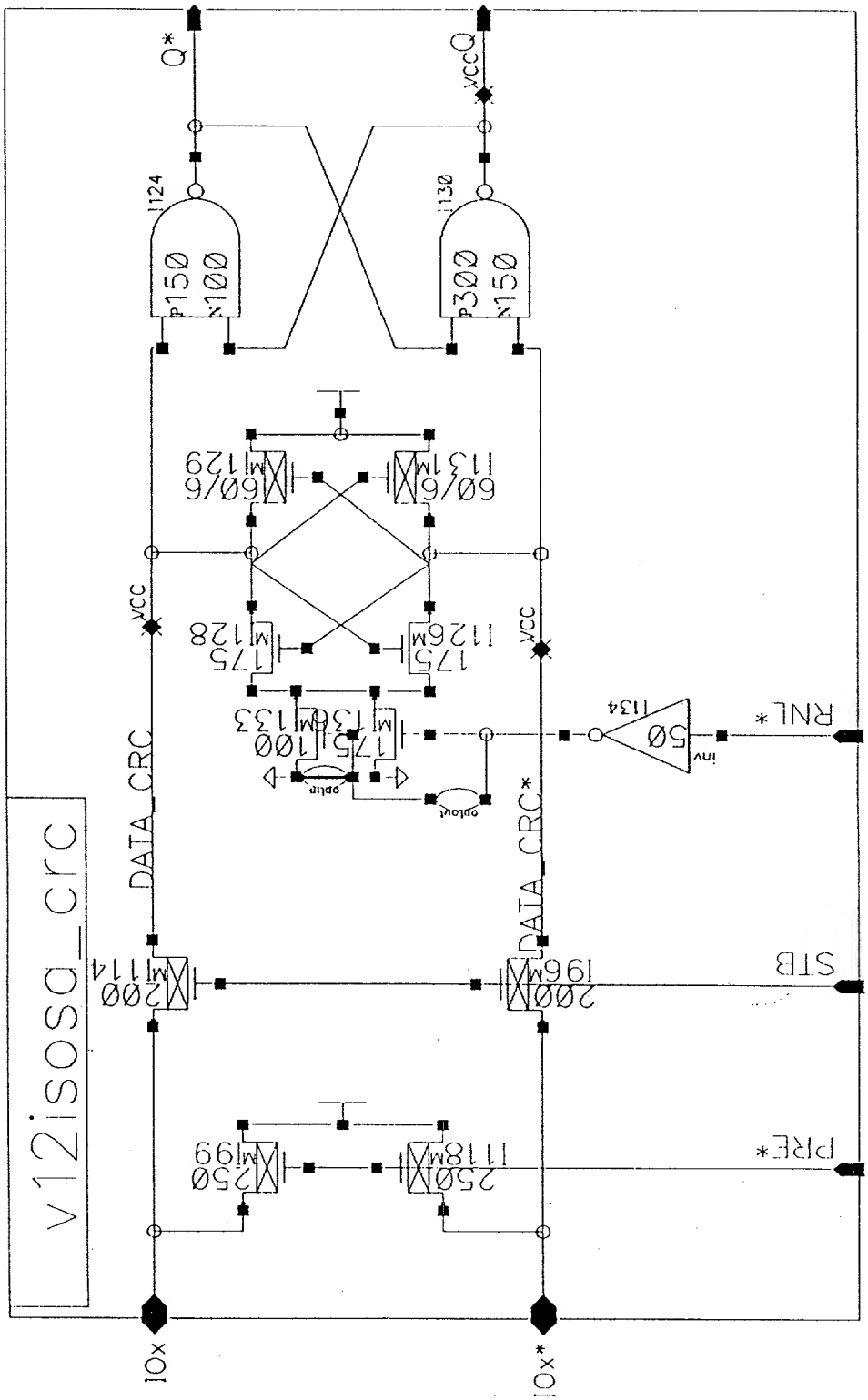

v12crc_comp
A
B
C
D
E
F
G
v12wr_drv_crc
Qx
EN
CRC_START
CRC_WRITE
CRCI<7:0>
CRCI*<7:0>
v12en_driver
D
D*
CLK
Q
CTLEN_OE
IO_OE
DQH
DQL
CRCDQH
CRCDQL
1=error, 0=match
CRCECC<7:0>

FIG. 5B

FIG. 6


v12isosa_crc
Q*
vccQ
1124
1130
P150
N100
P300
N150
60/6
1131M
M129
vcc
175
1126M
M128
175
100
1135M
M133
opbar
opbar
RNL*
1134
50
inv
DATA_CRC
DATA_CRC*
200
196M
M114
STB
250
1118M
M99
PRE*
IOx
IOx*

110

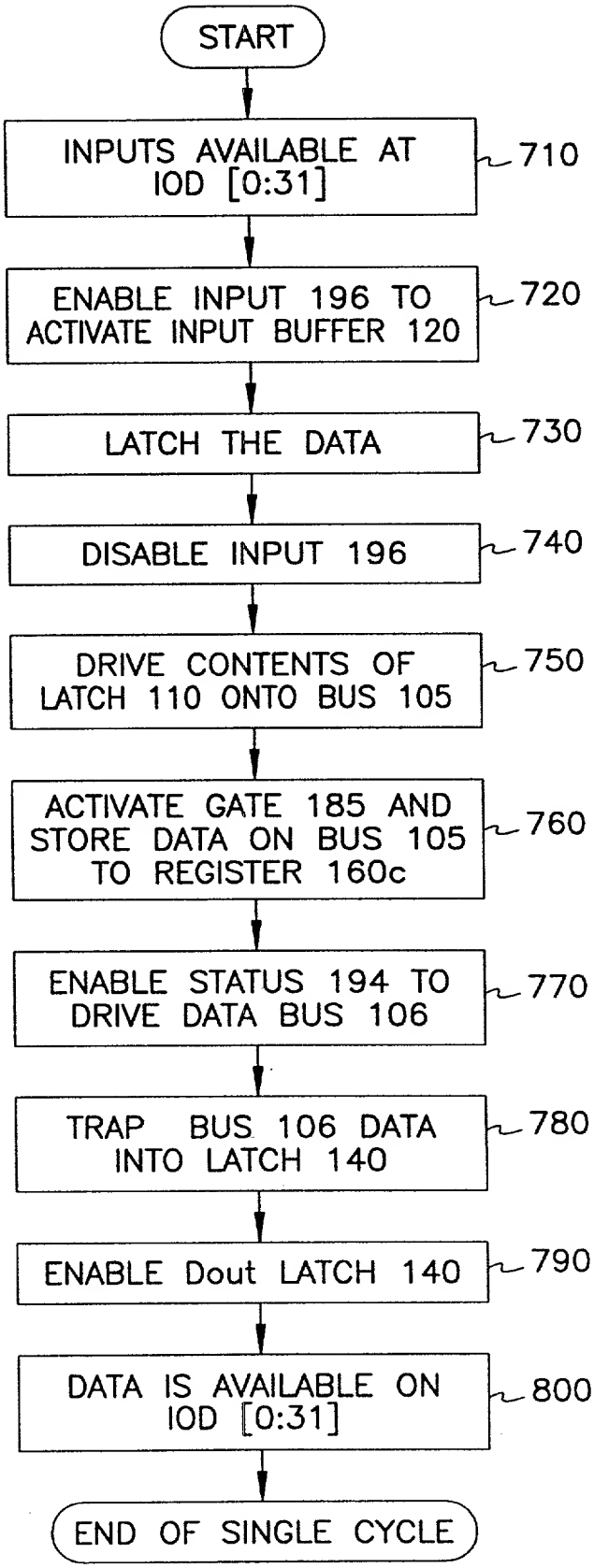

START
INPUTS AVAILABLE AT IOD [0:31]
710
ENABLE INPUT 196 TO ACTIVATE INPUT BUFFER 120
720
LATCH THE DATA
730
DISABLE INPUT 196
740
DRIVE CONTENTS OF LATCH 110 ONTO BUS 105
750
ACTIVATE GATE 185 AND STORE DATA ON BUS 105 TO REGISTER 160c
760
ENABLE STATUS 194 TO DRIVE DATA BUS 106
770
TRAP BUS 106 DATA INTO LATCH 140
780
ENABLE Dout LATCH 140
790
DATA IS AVAILABLE ON IOD [0:31]
800
END OF SINGLE CYCLE

FIG. 7

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: METHOD AND APPARATUS FOR A HIGH SPEED CYCLICAL REDUNDANCY CHECK SYSTEM.

The specification of which
a. __ is attached hereto
b. X was filed on June 7, 1995 as application serial no. 08/474,397 and was amended on __ (if applicable) (in the case of a PCT-filed application) described and claimed in international no. __ filed __ and as amended on __ (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

a. X no such applications have been filed.
b. __ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	**APPLICATION NUMBER**	**DATE OF FILING (day, month, year)**	**DATE OF ISSUE (day, month, year)**

ALL FOREIGN APPLICATIONS, IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	**APPLICATION NUMBER**	**DATE OF FILING (day, month, year)**	**DATE OF ISSUE (day, month, year)**

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

US APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS(patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

		Gebhardt, Mark J.	Reg. No. 35,518	Raasch, Kevin W.	Reg. No. 35,651
Billig, Patrick G.	Reg. No. 38,080	Kluth, Daniel J.	Reg. No. 32,146	Schwappach, Karl G.	Reg. No. 35,786
Brennan, Thomas F.	Reg. No. 35,075	Lemaire, Charles A.	Reg. No. 36,198	Schwegman, Micheal L.	Reg. No. 25,816
Clark, Barbara J.	Reg. No. 38,107	Lundberg, Steven W.	Reg. No. 30,568	Viksnins, Ann S.	Reg. No. 37,748
Forrest, Bradley A.	Reg. No. 30,837	Mueting, Ann M.	Reg. No. 33,977	Woessner, Warren D.	Reg. No. 30,440

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/ firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, & Woessner, P.A. to the contrary.

Please direct all correspondence in this case to Schwegman, Lundberg & Woessner, P.A. at the address indicated below:
3500 IDS Center, Minneapolis, MN 55402
Telephone No. (612)339-0331

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

201	Full Name of Inventor	Family Name	First Given Name	Second Given Name
		Thomann	Mark	
	Residence & Citizenship	City	State or Foreign Country	Country of Citizenship
		Boise	Idaho	USA
	Post Office Address	Post Office Address	City	State & ZipCode/Country
		P. O. Box 5006	Boise	Idaho 83704/USA
202	Full Name of Inventor	Family Name	First Given Name	Second Given Name
		Vo	Huy	Thanh
	Residence & Citizenship	City	State or Foreign Country	Country of Citizenship
		Boise	Idaho	USA
	Post Office Address	Post Office Address	City	State & ZipCode/Country
		2463 E. Red Cedar Lane #103	Boise	Idaho 83705/USA
203	Full Name of Inventor	Family Name	First Given Name	Second Given Name
		Ingalls	Charles	L.
	Residence & Citizenship	City	State or Foreign Country	Country of Citizenship
		Meridian	Idaho	USA
	Post Office Address	Post Office Address	City	State & ZipCode/Country
		982 West Pennwood	Meridian	Idaho 83642/USA

Signature of Inventor 201	Signature of Inventor 202	Signature of Inventor 203
	Huy Thanh Vo	Charles L Ingalls
Date 8-10-95	Date 8/10/95	Date 8-10-95

For Additional Inventors: __ Indicate here and attach sheet with same information, including date and signature.

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.